TCET/FRM/IP-02/10 Revision: B

Semester Plan
(Practical / tutorials / Assignment)

Semester: **BE - VII** Course: **B.E ETRX** Batches:

Subject: **IC Technology Laboratory (EXL702)** Class: **B.E ETRX** Batch Size: **20 students**

Laboratory faculty In-Charge: **Mr. Sunil Khatri,Mr. Sumit K** Lab Assistant / Attendant: **Ms. Sulbha Kashid**

Note: **Experiments are planned as per University Curriculum**

Basic Experiments

Sr. No	TITLES Experiments / Tutorials / Assignment (Planning with use of Technology)	Planned Date	Completion Date	Remarks
1	To use Hall effect to find semiconductor type, conductivity and carrier concentration	**E1, E2 : 25/7**		
		E3, E4 : 24/7		
2	To study CMOS fabrication process using N well	**E1, E2 : 1/8**		
		E3, E4 : 31/7		
3	To study output characteristics of MOSFET using TCAD	**E1, E2 : 8/8**		
		E3, E4 : 7/8		
4	To study SOI and its characteristics using TCAD	**E1, E2 : 5/9**		
		E3, E4 : 14/8		

Design / Development Experiments:

Sr. No	TITLES Experiments / Tutorials / Assignment (Planning with use of Technology)	Planned Date	Completion Date	Remarks
5	Design and implementation of CMOS inverter layout	**E1, E2 : 12/9**		
		E3, E4 : 21/8		
6	Design and implementation of NAND gate layout	**E1, E2 : 19/9**		
		E3, E4 : 4/9		
7	Design and implementation of NOR gate layout	**E1, E2 : 26/9**		
		E3, E4 : 11/9		
8	Perfomance parameters Testing of CMOS inverter with change in technology trends	**E1, E2 : 3/10**		
		E3, E4 : 18/9		
9	Design a NMOS current mirror circuit and testing it with change in technology trends	**E1, E2 : 10/10**		
		E3, E4 : 25/9		
10	Design a transmission gate circuit and testing it in terms of process parameters	**E1, E2 : 17/10**		
		E3, E4 : 9/10		

Group Learning Activity

1	**Mini Project:** Design a Wilson current mirror circuit and testing it in terms of process parameters	**E1, E2**		
2	**Mini Project:** Design a Cascode current mirror circuit and testing it in terms of process parameters	**E3, E4**		
3	**Case study:** Different multigate devices and its applications, (SOI,CINFET, FINFET,MESFET,HEMT)	**E1, E2, E3, E4**		

Mini / Minor Projects Objective: To get hands on experience to execute projects with respect to student choice in the following areas. (**30 Hrs / Semester / Student**).

The areas are :
1. Research 2. Core 3. Interdisciplinary 4. Application

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Mini /Minor Projects :

S.No	Project Title	Class	Group Size/ Project Hours	Project Type	Reference
1	Double gate CINFET	BE	3-4	Major	Technology Based Learning
2	Simulation of High Electron Mobility Transistor,SOIFET	BE	3-4	Major	

	Planned	Completed		Planned	Completed		Planned	Completed	
No. of Prac	**Basic Exp:** 04 **Design Base Exp**: 06 **Major Project:** 2 **Case study:** 2(any)		No. of Assignments	3		No. of Tutorial	01(Low Profile Student)		

DOSLNE:	DOSLE (engaged in some other dates):

Group activities are required to be added with the practical related to course to enhance the learning activity of the student in the course. Group activity includes: Group presentation, new experiment design, mini projects etc.

Note:

1. The practical plan date and completion date shall be in compliance. For any non-compliance reason(s) required to be stated in remark column.
2. Learning objective and outcome shall be clearly stated with each of experiments/ tutorials/ assignments and are required to be mapped at the end of the semester.
3. Entry for DOSLE (engaged on some other date) shall be done with proper mapping to DOSLNE.

Name & Signature of Faculty Signature of HOD Signature of Principal / Dean Academic

Date: 11/01/2017 Date: Date: